(Please write your Exam Roll No.)

Exam Roll No. .....

## END TERM EXAMINATION

First Semester [MCA] December-2009

Paper Code: MCA103 Subject: Digital Electronics Paper Id-44103		
Tin	ne : 3 Hours Maximum Marks: 60	
	Note: Q.1 is compulsory. Attempt one question from each unit.	
Q1	Answer the following questions:- (2x10= (a) Convert 111011 into hexadecimal through octal. (b) What are the advantages of Gray code? (c) Write down fan in and fan out of standard TTL ICs	20)
	<ul><li>(d) Represent the logic diagram of the half adder.</li><li>(e) What is the drawback of the SR Flip Flop and how is it minimized?</li><li>(f) What is a sequence generator?</li></ul>	
	<ul> <li>(g) What is asynchronous sequential circuit?</li> <li>(h) Draw a scale of 8 ripple counter.</li> <li>(i) What do you mean by static and dynamic memories?</li> <li>(i) How is an individual location in EEPROM erased or modified?</li> </ul>	
Q2	(a) Prove the following by perfect induction method. (i) A+AB=A (ii) A(A+B)=A (iii) A+A'B=A+B (iv) A(A'+B)=AB (b) Peduce the function function function for and realize it using NAND setes only.	(4)
	(b) Reduce the function 1 using K-map and realize it using NAND gates only. f = ABC' + A'B'C + ABC + AB'C <b>OR</b>	(6)
Q3	(a) Minimize the function using Boolean algebra $f = x(y+w'z) + wxz$ .	(4)
	(b) Design a 2 input NAND gate using 2:1 multiplexer.	(3)
	(c) Draw the logic diagram of 4-bit universal shift register.	(3)
~	UNIT-II	
Q4	Design synchronous counter that counts in the sequence 0,2,6,1,7,5 and 0 using D-FFs.	(10)
	Draw the logic diagram and state diagram.	(10)
05	Draw the circuit diagrams of 2 input CMOS NOR gate and CMOS NANA gate using	
Q2	CMOS logic and explain their operation.	(10)
	<u>UNIT-III</u>	, í
Q6	(a) Write short notes on races and cycles that occur in fundamental circuits.	(3)
	(b) What is an essential hazards? Explain with example.	(3)
	(c) Explain how hazard free realization can be obtained for a Boolean function?	(4)
Q7	OR Draw an asynchronous decade counter and explain its operation by drawing waveforms. UNIT-IV	(10)
Q8	Explain Instruction cycle and Interrupt cycle with the help of flowchart. Describe instruction format and addressing mode bits.	(10)
00	OR Line Line Construction of Line Line Line Line Line Line Line Line	
Q9	A microprocessor multiplexes data from four different data terminals and sends the	
	inumprexed data over a telephone link to a remote unit, via a UAK1. Suggest the most suitable $I/O$ communication scheme (such as parallel social synchronous, estimated as	
	strobed, handshaked) between :- ((	(10)
	(a) The microprocessor and the UART	
	(c) The $IIAPT$ and the remote unit	
	(c) The OART and the femote unit. *******	