

(Please write your Exam Roll no)

Exam Roll No.....

END TERM EXAMINATION

SECOND SEMESTER [MCA] MAY-2010

Paper Code: MCA 106

Subject: Computer System Architecture

Paper ID:44106

Time: 3 Hours

Maximum Marks: 60

Note: Question 1 is Compulsory. Attempt one question from each unit.

Q-1 Explain in brief:

(6X2=12)

- (a) List the five generations of evolution of computers.
- (b) What are the differences between MAR & MBR?
- (c) List '6' types of addressing modes used in Computer Architecture.
- (d) List the differences between direct memory and associative memory.
- (e) List the differences between Microprogramming and macro programming.
- (f) List the differences between RISC and CISC machine.

UNIT-I

Q-2(a) Construct a 5-to-32 line decoder with four 3-to-8-line decoders with enable and one 2-to-4 decoder.(6)

(b) Consider a memory chip (RAM) of 4096X32 size .Draw a block diagram and label all input and output terminals in the RAM. Also give the answer of the following questions(6)

I) how many address lines are there in this chip?

(ii) How many data lines are there in the chip?

(iii) What is the word size of the RAM chip?

(iv) What is the capacity of RAM chip in bytes?

Q-3 (a) what is a BUS in the context of Computer Architecture? Draw the logic diagram of a 4 bit bus involving 2 input and 2 output registers using multiplexer.(6)

(b) What is a micro operation? How is it different from an instruction of a computer? Explain the steps of 'instruction fetch' and interrupt 'Processing' .(6)

UNIT-II

Q-4(a) Consider an initial value of R as 11011011, determine the sequence of binary values in R after a logical shift-left followed by circular shift right, followed by a logical shift-left, and an arithmetic shift-right operations are performed on the register. Show the value after each operation.(6)

(b) Differentiate between a branch instruction, a call subroutine instruction and program interrupt.(6)

Q-5(a) Differentiate between direct and indirect address instructions? How many memory references are required for each type of instruction to bring an operand into a processor register? Explain.(6)

(b) Convert the given arithmetic expression from infix to reverse polish notation $A+B*[C*D+E*(F+G)]$ (3)

(c) Convert the given arithmetic expression from reverse Polish notation to infix. $ABC*/D-EF/+$ (3)

UNIT-III

Q-6(a) what is a vector instruction? How does array processor help in execution of Vector Instruction?(5)

(b) Draw a flowchart for adding and subtracting 2 fixed point binary numbers when the negative numbers are in signed 1's complement representation.(7)

Q-7(a) Describe the basic operation to be performed for the division of 2 floating point numbers. Give a flowchart for that Floating point division depicting the basic operation.(6)

(b) Show that there can be no mantissa overflow after a multiplication operation.(6)

UNIT-IV

Q8 Differentiate between the following:

(a) Memory mapped I/O and isolated I/O. (6)

(b) Associative cache mapping and Set Associative cache mapping. (6)

Q-9 Write short notes on any three of the following: (4X3=12)

(a) Segmented Page Mapping

(b) Differentiate between DMA and IOP.

(c) Memory reference instruction

(d) Logic Micro-operations.

